CLAIM AMENDMENT:

Please amend Claims 1, 5, 8, 11, 12, 13, 20 and 25, and add new claims 29-36 as follows:

Claim 1 (currently amended): A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a first internal circuit on the insulating substrate, the first semiconductor chip having a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad, and the conductive relay pad including a first area and a second area, which is different from the first area;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a first bonding wire connecting the first terminal pad to the first conductive pattern;

a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area; and

a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad;

wherein the lengths of the first, second and third bonding wire are approximately

the same.

Claim 2 (original): A multi-chip package type semiconductor device, as claimed in claim 1, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 3 (previously amended) A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a first metal bump formed on the conductive relay pad in the first area and a second metal bump formed on the second terminal pad, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern, wherein a first bond as a beginning connection of the second bonding wire is preformed at the second conductive pattern and a second bond as an ending connection of the second bonding wire is made at the first metal bump, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the conductive relay pad in the second area and a second bond as an ending connection of the third bonding wire is made at the second metal bump.

Claim 4 (previously amended): A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a metal bump formed on the conductive relay pad in the second area, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern,

wherein a first bond as a beginning connection of the second bonding wire is preformed at the conductive relay pad in the first area and a second bond as an ending connection of the second bonding wire is made at the second conductive pattern, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the second terminal pad and a second bond as an ending connection of the third bonding wire is made at the metal bump.

Claim 5 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 6 (previously amended): A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 7 (original): A multi-chip package type semiconductor device, as claimed in claim 6, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claim 8 (currently amended). A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 9 (previously amended): A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 10 (original): A multi-chip package type semiconductor device, as claimed in claim 9, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claim 11 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 3, wherein the first metal bump is spaced apart from ~~not physically connected to~~ the first bond of the third bonding wire, but is electrically connected to the first bond of the third bonding wire via the conductive relay pad.

Claim 12 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 4, wherein the metal bump is spaced apart from ~~not physically connected to~~ the first bond of the second bonding wire, but is electrically connected to the first bond of the second bonding wire via the conductive relay pad.

Claim 13 (currently amended): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first terminal pad and a conductive relay pad, the conductive relay pad including a first area and a second area, which is different from the first area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a second terminal pad, connected to the conductive relay pad in the second area;

a first internal terminal connected to the first terminal pad; and

a second internal terminal connected to the conductive relay pad in the first area.

Claim 14 (original): A multi-chip package type semiconductor device, as claimed in claim 13, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 15 (original): A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor

chip having a first internal circuit, a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a first bonding wire connecting the first terminal pad to the first conductive pattern;

a second bonding wire connecting the second conductive pattern to the conductive relay pad; and

a third bonding wire connecting the conductive relay pad to the second terminal pad;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 16 (original): A multi-chip package type semiconductor device, as claimed in claim 15, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 17 (previously amended): A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a first metal bump formed on the conductive relay pad and a second metal bump formed on the second terminal pad, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first

bonding wire is made at the first conductive pattern, wherein a first bond as a beginning connection of the second bonding wire is preformed at the second conductive pattern and a second bond as an ending connection of the second bonding wire is made at the first metal bump, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the first metal bump and a second bond as an ending connection of the third bonding wire is made at the second metal bump.

Claim 18 (previously amended): A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a metal bump formed on the conductive relay pad, wherein a first bond as a beginning connection of the first bonding wire is preformed at the first terminal pad and a second bond as an ending connection of the first bonding wire is made at the first conductive pattern, wherein a first bond as a beginning connection of the second bonding wire is preformed at the conductive pattern and a second bond as an ending connection of the second bonding wire is made at the metal bump, and wherein a first bond as a beginning connection of the third bonding wire is preformed at the second terminal pad and a second bond as an ending connection of the third bonding wire is made at the metal bump.

Claim 19 (previously added): A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 20 (currently amended): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first conductive portion and a second conductive portion, the second conductive portion having a first area and a second area, which is different from the first area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion, connected to the second conductive portion in the first area;

a first internal terminal connected to the first conductive portion; and

a second internal terminal connected to the second conductive portion in the second area.

Claim 21 (previously added): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 22 (previously added): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 23 (previously added): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are spaced from each other.

Claim 24 (previously added): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising:

a bump formed on the second conductive portion in the second area; and

a first wire, the first wire having one end connected to the second terminal and the other end connected to the bump.

Claim 25 (currently amended): A multi-chip package type semiconductor device, comprising:

an insulating substrate;

a first conductive pattern formed on the insulating substrate;

a first semiconductor chip mounted on the insulating substrate;

a second conductive pattern formed on the first semiconductor chip, the second conductive pattern having a first area and a second area, which is different from the first area;

a second semiconductor chip mounted on the first semiconductor chip;

a third conductive pattern formed on the second semiconductor chip;

a first wire connected between the first area of the second conductive pattern and the third conductive pattern; and

a second wire connected between the second area of the second conductive pattern and the first conductive pattern.

Claim 26 (previously amended): A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second areas are located along a side of the first semiconductor chip.

Claim 27 (previously added): A multi-chip package type semiconductor device, as claimed in claim 25, further comprising:

a first bump formed on the first area of the second conductive pattern; and

a second bump formed on the third conductive pattern,

wherein the first wire is connected to the first area through the first bump and the second wire is connected to the third conductive pattern through the second bump.

Claim 28 (previously added): A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second area are spaced each other.

Claim 29 (new): A multi-chip package type semiconductor device, as claimed in claim 1, further comprising a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned.

Claim 30 (new): A multi-chip package type semiconductor device, as claimed in claim 1, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claim 31 (new): A multi-chip package type semiconductor device, as claimed in claim 13, further comprising a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned.

Claim 32 (new): A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claim 33 (new): A multi-chip package type semiconductor device, as claimed in claim 15, further comprising a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned.

Claim 34 (new): A multi-chip package type semiconductor device, as claimed in claim 15, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claim 35 (new): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising a plurality of first conductive portions and a plurality of second conductive portions, wherein each first conductive portion and each second conductive portion are alternatively aligned.

Claim 36 (new): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first conductive portion is rectangularly-shaped, and a side of the first conductive portion is parallel to the side of the first semiconductor chip.

REMARKS

The Examiner's Office Action mailed May 21, 2003 has been received and carefully reviewed. Claims 1, 5, 8, 11, 12, 13, 20 and 25 have been amended and no claims have been canceled. Further, new claims 29-36 are added. Therefore, claims 1-36 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

Initially, it is noted that this Amendment increases the total number of claims pending in the application to thirty six (36) from twenty eight (28), thus requiring an excess claim fee of $144.00 for eight (8) claims. It is further noted that this Amendment does not increase the total number of independent claims pending in the application. Thus, a fee of $144.00 for eight (8) claims in excess is required. Please charge the necessary fee of $144.00 to our Deposit Account No. 50-0945.

In the action, claims 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification. Specifically, the examiner asserts that the non-described subject matter is the claim 11 limitation, wherein the first metal bump is not physically connected to the first bond of the third bonding wire, and the claim 12 limitation, wherein the second area is not physically connected to the first bond of the second bonding wire. Further, the examiner asserts additionally that the bumps are electrically but not physically connected to the bonds via the conductive relay pad appear to be incorrect because it appears that electrical connection requires physical connection. **Applicant disagrees.** "being not physically contented" means "no physical contact". Nevertheless, Applicant

has amended claims 11 and 12 in order to make a meaning of the limitation clear so the rejection is no longer applied to these claims.

In the Action, claims 13, 14, 19-23, 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Takiar, or in alternative, under 35 U.S.C. 103(a) as obvious over Takiar in combination with O'Conner.

First of all, independent claims 1, 13, 20 and 25 are amended to make claim limitations clear wherein a first area is different from a second area. According to this amendment, the examiner's misunderstanding of these claims will be resolved.

As the examiner admitted in the Action on page 7, line 17 through page 8, line 3, Takiar does not disclose the limitations which are a conductive relay pad including a first area and a second area, a second terminal pad connected to the conductive relay pad in the second area, a second internal terminal connected to the conductive relay pad in the first area, a first wire connected between the first area of the second conductive pattern and the third conductive pattern and a second wire connected between the second area of the second conductive pattern and the first conductive pattern. Further, as explained in the Paper on page 7, lines 3-10, filed February 11, 2003, Takiar does **not** disclose that an electrical contact (58) includes a first area and a second area. Takiar simply discloses that an electrical contact (54) and an electrical lead (44) are connected to the electrical contact (58). Since the electrical contact (58) does not has a first area and a second area, it is not, of course, disclosed that the electrical contact (54) and the electrical lead (44) are connected to the first and the second areas of the electrical contact (58), respectively. As a result, according to Takiar, stress of wire bonding (56), (60) on the electrical contact can **not** be reduced.

The examiner assets even if Takiar does not disclose above-described characteristics, O'Conner teaches them. **However, the U.S. filing date of the present invention was one day earli r than that of the O'Conner referenc .** Applicant respectfully requests to show the legal basis that O'Conner can be applied to the present invention as prior art. Otherwise, Applicant respectfully requests to withdraw this rejection.

In the Action, claims 23, 24, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar and O'Conner.

As described above, **the U.S. filing date of the present invention was one day earlier than that of the O'Conner reference.** Applicant respectfully requests to show the legal basis that O'Conner can be applied to the present invention as prior art. Otherwise, Applicant respectfully requests to withdraw this rejection. Further, it is noted that claim 28 has not rejected by other basis in the Action.

In the Action, claims 1, 2, 15 and 16 are rejected under 35 U.S.C. 103(a) as obvious over Takiar or combination of Takiar and Haba, or combination of Takiar and O'Conner, or or combination of Takiar, Haba and O'Conner.

As the examiner admitted in the Action on page 12, lines 1 - 6, Takiar does not disclose the limitations which are a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area, and a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad. Further, as explained in the Paper on page 7, lines 3-10, filed February 11, 2003, Takiar does **not** disclose that the conductive relay pad having the first arean and teh

second area as descried above, and any electrical contacts formed on a semiconductor die (22), which are connected **only** to an electrical lead (44). In other words, Takiar does not disclose any wires corresponding to the first bonding wire of the invention.

The examiner assets even if Takiar does not disclose above-described characteristics, O'Conner teaches them. **However, the U.S. filing date of the present invention was one day earlier than that of the O'Conner reference.** Applicant respectfully requests to show the legal basis that O'Conner can be applied to the present invention as prior art. Otherwise, Applicant respectfully requests to withdraw this rejection.

Moreover, the examiner also admitted in the Action on page 12, lines 13-15, that Takiar does not disclose the limitation which is the lengths of the first, second and third bonding wire being approximately the same. However, the examiner assets that this limitation is an obvious matter of design choice. **Applicant disagrees**. As explained in the Paper on page 9, line 21 through page 10, line 2, and page 8, lines 8-13, filed February 11, 2003, since all lengths of the bonding wire are approximately the same, it is possible to avoid unnecessary contact of the bonding wires, which are next to each other when the semiconductor device is encapsulated by a sealing material (Refer to the specification on page 8, lines 11-20). The examiner has never rebutted to this remark.

The examiner also assets that Haba teaches the limitation regarding the lengths of the first, second and third bonding wire, repeatedly. However, as explained in the Paper on page 9, lines 9-21, filed February 11, 2003, the bonding wire 440a of Haba does not correspond to the first bonding wire of the invention. The bonding wire 440a corresponds to the second bonding wire of the invention, and the bonding wire 440b of

Haba corresponds to the third bonding wire of the invention. In other words, Haba does not disclose the first bonding wire of the invention. The examiner has never rebutted to this remark.

In the Action, claims 3-12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar and O'Conner or the combination of Takiar, Haba and O'Conner.

As described above, **the U.S. filing date of the present invention was one day earlier than that of the O'Conner reference.** Applicant respectfully requests to show the legal basis that O'Conner can be applied to the present invention as prior art. Otherwise, Applicant respectfully requests to withdraw this rejection.

Specifically, the examiner admitted in the Action on page 17, line 17 though page 18, line 4, Takiar does not disclose the limitations claimed in claim 7 and 10. It is noted that claims 7 and 10 have not rejected by other basis in the Action.

In the Action, claims 5, 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar and O'Conner, or the combination of Takiar, Haba and O'Conner, and further in combination with Hill.

As described above, **the U.S. filing date of the present invention was one day earlier than that of the O'Conner reference.** Applicant respectfully requests to show the legal basis that O'Conner can be applied to the present invention as prior art. Otherwise, Applicant respectfully requests to withdraw this rejection.

It is noted that this Amendment has been prepared using the requested new format. If there are any irregularities in this format, it would be greatly appreciated if Applicant's Counsel would be so advised

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any fee be further needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Respectfully submitted

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Date : July 30, 2003